2819/4

ATENT APPLICATION

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AMENDMENT TRANSMITTAL

In re the Application of

Akihiko EBINA et al.

Group Art Unit: 2814

Application No.: 10/052,549

Examiner:

M. Pizarro Crespo

Filed:

January 23, 2002

For:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING NONVOLATILE

SEMICONDUCTOR MEMORY DEVICES

Director of the U.S. Patent and Trademark Office

Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

Entitlement to small entity status is hereby asserted.

Small entity status of this application has been established.

The filing fee has been calculated as shown below:

	(Column 1)	(Column 2)	(Column 3)	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	
TOTAL CLAIMS	*19 MINUS	**20	=	
INDEP CLAIMS	*4 MINUS	***3	=1	
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY			
RATE	ADD'L FEE		
x 9	s		
x 42	\$		
+140	\$		
	\$		

- * If the entry in Column 1 is less than the entry in Column 2, write "0" in Column 3.
- ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.
- *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" in this space (Total or Independent) is the highest number found from the equivalent box in Column 1 of a prior Amendment or the number of claims originally filed.

Check No. 139609 in the amount of \$84.00 is attached. The Director is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 15-0461. Two duplicate copies of this sheet are attached.

Respectfully submitted,

James A. Oliff

Registration No. 27,075

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JAO:GPS/can

Date: March 3, 2003



PATENT APPLICATION

M. Pizarro Crespe

1117**7**

Group Art Unit: 2814

Examiner:

Docket No.:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Akihiko EBINA et al.

Application No.: 10/052,549

Filed: January 23, 2002

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING

NONVOLATILE SEMICONDUCTOR MEMORY DEVICES

AMENDMENT UNDER 37 C.F.R. §1.111

Director of the U.S. Patent and Trademark Office Washington, D.C. 20231

Sir:

In reply to the December 3, 2002 Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please replace claim 7 as follows:

7. (Amended) The semiconductor integrated circuit device as defined in claim 1, wherein:

a buried insulating layer is formed between the two side insulating layers disposed in contact with the first and second control gates; and

the buried insulating layer covers the adjacent first and second control gates.

Please add new claims 13-19 as follows:

--13. A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

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